UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,991	07/29/2003	John T. Stonick	SNPS-0254	7681

36503 7590 03/20/2007

SYNOPSYS, INC
c/o PARK, VAUGHAN & FLEMING LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

EXAMINER	
BENGHUZZI, MOHSIN M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,991	STONICK ET AL.	
	Examiner	Art Unit	
	Mohsin (Ben) Benghuzzi M.B.	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *December 22, 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *January 12, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 5, 17, and 19 have been considered but are moot in view of the new ground of rejection due to the amendment.

Applicant's argument - "There is nothing within Tang, Davis, Little, or Ma, either separately or in concert, which suggests providing margining circuitry to determine the value of an error signal of a level sampling point." (Second paragraph, response to Rejections under 35 U.S.C. §102(b) and §103(a), page 11).

Examiner's response - Applicant has not pointed out distinctly in the language of the claims what specific reference value, i.e., 'level', the cited error signal is measured against. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Therefore, examiner has interpreted the value of the error signal in the claims to be measured against a voltage reference level, i.e., examiner has interpreted the 'level sampling point' to be a voltage reference level. Thus, Applicant's argument that Tang, Davis, Little, or Ma do not suggest providing margining circuitry to determine the value of an error signal of a level sampling point is moot, as Ma et al. does disclose a margining circuitry to determine the value of an error signal of a level sampling point (Paragraphs 25, 42, paragraph 43 lines 8-13 and 70 in Fig. 5, wherein, 70 in Fig. 5 is interpreted as the margining circuitry and the 'tracking error signal TES' is interpreted as the value of an error signal of a level sampling point).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 5, 17, and 19, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant has not pointed out distinctly in the language of the claim what specific reference value, i.e., level, the cited error signal is measured against.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (US Pub 2002/0075012) in view of Ma et al. (US Pub 2002/0094024).

1) Regarding claim 1:

Tang et al. discloses an equalization circuit to receive a plurality of input symbols and to generate an output signal wherein the output signal is representative of a transmitted symbol (100 in Fig. 1), the equalization circuit comprising:

a first data slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first data slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level (120 in Fig. 1, Paragraph 17 Lines 1-4, Table 1 Page 2, Paragraphs 19 and 20);

a second data slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level (130 in Fig. 1, Paragraph 17 Lines 1-4, Table 1 Page 2, Paragraphs 19 and 20); and

logic circuitry, coupled to the first and second data slicers, to output a signal having either a first or second logic level wherein the first logic level is associated with the first value and the second logic level is associated with the second logic level (140 in Fig. 1), and wherein:

if the data slicers output the same value, the logic circuitry outputs the logic level that is associated with the value output by the data slicers (Table 1 Page 2, wherein, when inputs '142' and '144' in Fig. 1 are the same is interpreted as when the data slicers output the same value); and

if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol (Table 1 Page

2, wherein, when inputs '142' and '144' in Fig. 1 are different is interpreted as when the data slicers output different values).

Tang et al. does not disclose, margining circuitry to measure the value of an error signal of a level sampling point. However, Ma et al. discloses, margining circuitry to measure the value of an error signal of a level sampling point (Paragraphs 25, 42, paragraph 43 lines 8-13 and 70 in Fig. 5, wherein, 70 in Fig. 5 is interpreted as the margining circuitry and the 'tracking error signal TES' is interpreted as the value of an error signal of a level sampling point).

It is desirable to use a margining circuitry to measure the value of an error signal of a level sampling point. The error signal produced by the margining circuitry can be used in a feedback fashion to control and reduce the error in the input signal that is to be detected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the equalization circuit of Tang et al. a margining circuitry to measure the value of the error signal of the level sampling point, as Ma et al. teaches, in order to be able to reduce the error in the input signal that is to be detected.

2) Regarding claim 2:

Tang et al. discloses the equalization circuit of claim 1 wherein the first and second data slicers each include at least one voltage comparator (Pages 3-4 claim 1 Lines 8-13).

3) Regarding claim 3:

Tang et al. discloses the equalization circuit of claim 2 wherein the first and second data slicers each include a plurality of serially coupled sense amplifiers (Paragraph 17 Lines 4-6).

4) Regarding claim 4:

Tang et al. discloses the equalization circuit of claim 1 further including adaptive circuitry, coupled to the first data slicer, to determine the first slicer level during operation of the equalization circuit and to provide the first slicer level to the first data slicer (Paragraph 16 Lines 4-7 and Paragraph 20 Lines 1-3).

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (US Pub 2002/0075012) and Ma et al. (US Pub 2002/0094024), and further in view of Davis et al. (US 6,505,222).

1) Regarding claim 5:

Tang et al. discloses a receiver, coupled to a communications channel, to receive a plurality of input symbols transmitted by a transmitter, and to generate an output signal that is representative of each transmitted symbol (Paragraph 5 Lines 1-4 and Paragraph 16 Lines 3-4), the receiver comprising:

equalization circuitry, coupled to the communications channel to receive the plurality of input symbols (100 in Fig. 1), the equalization circuitry including:

a first data slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted

to receive a first slicer level, and wherein the first data slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level (120 in Fig. 1, Paragraph 17 Lines 1-4, Table 1 Page 2, Paragraphs 19 and 20);

a second data slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level (130 in Fig. 1, Paragraph 17 Lines 1-4, Table 1 Page 2, Paragraphs 19 and 20);

logic circuitry, coupled to the first and second data slicers, to output a signal having either a first or second logic level wherein the first logic level is associated with the first value and the second logic level is associated with the second logic level (140 in Fig. 1), and wherein:

if the data slicers output the same value, the logic circuitry outputs the logic level that is associated with the value output by the data slicers (Table 1 Page 2); and

if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol (Table 1 Page 2).

As discussed in claim 1 above, Ma et al. discloses, margining circuitry to measure the value of an error signal of a level sampling point (Paragraphs 25, 42, paragraph 43 lines 8-13 and 70 in Fig. 5, wherein, 70 in Fig. 5 is interpreted as the

margining circuitry and the 'tracking error signal TES' is interpreted as the value of an error signal of a level sampling point).

Tang et al. or Ma et al. do not disclose, a memory, coupled to the second input of each data slicers, wherein the memory stores information which is representative of the first and second slicer levels. However, Davis et al. discloses, a memory, coupled to the second input of each data slicers, wherein the memory stores information which is representative of the first and second slicer levels (Column 11 Lines 23-29).

It is desirable to store information representative of a first and second slicer levels of two slicers. Storing information representative of slicer levels prevents the information from having to be regenerated each time the levels are needed for comparison with first slicers' inputs. This results in an equalization circuit that is faster and more efficient. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a memory for storing information representative of the first and second slicer levels, as Davis et al. discloses, in the receiver of Tang et al. and Ma et al., in order to result in an equalization circuit that is faster and more efficient.

2) Regarding claim 6:

Tang et al. discloses receiver of claim 5 further including adaptive circuitry, coupled to the second input of each data slicers, wherein the adaptive circuitry adjusts the first and second slicer levels in accordance with the performance of the receiver (Paragraph 16 Lines 4-7 and Paragraph 20 Lines 1-3).

7. Claims 7-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (US Pub 2002/0075012), Ma et al. (US Pub 2002/0094024), Davis et al. (US 6,505,222), and further in view of Little (US Pub 2003/0081697).

1) Regarding claim 7:

Tang et al., Ma et al., or Davis et al. do not disclose, further including adaptive circuitry, coupled to the second input of the first data slicer, wherein the adaptive circuitry changes the first data slicer level based on an upper edge and a lower edge of a receive eye of the first data slicer. However, Little discloses, further including adaptive circuitry, coupled to the second input of the first data slicer, wherein the adaptive circuitry changes the first data slicer level based on an upper edge and a lower edge of a receive eye of the first data slicer (Paragraph 40 Lines 1-8 and Paragraph 44 Lines 1-11).

It is desirable that a slicer level of a data slicer in a receiver is adaptively changed based on an upper edge and a lower edge of a receive eye of the data slicer. Including adaptive circuitry for changing slicer level will result in a data slicer with a slicer level that is optimized for symbol detection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include adaptive circuitry that changes the first data slicer level based on an upper edge and a lower edge of a receive eye of the first data slicer, as Little discloses, in the equalization circuitry of Tang et al., Ma et al., and Davis et al., in order to have a data slicer that is optimized for symbol detection.

2) Regarding claim 8:

Little further discloses, further including margining circuitry, coupled to the adaptive circuitry, wherein the margining circuitry determines the upper inner edge and the lower inner edge of the receive eye of the first data slicer (Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the margining circuitry, and the inner edges are interpreted as the upper and lower inner edges of the receive eye).

3) Regarding claim 9:

Little further discloses, wherein the margining circuitry includes a margining slicer having a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the margining circuitry, and the mid point between inner edges is interpreted to be the margining slicer level).

4) Regarding claim 10:

Little further discloses, wherein the margining circuitry includes reference level adjustment circuitry to generate the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the reference level adjustment circuitry).

5) Regarding claim 11:

Little further discloses, wherein the reference level adjustment circuitry generates margining slicer levels that vary according to the margining algorithm (Block 640 in Figs. 6, 7 and Paragraph 44 Lines 1-11, wherein, it is clearly understood that the margining algorithm is executed by the adaptive slicer threshold generation system).

6) Regarding claim 12:

Tang et al., Ma et al., or Davis et al. do not disclose, further including adaptive circuitry, coupled to the second input of the second slicer, wherein the adaptive circuitry changes the second slicer level based on an upper edge and a lower edge of a receive eye of the second slicer. However, Little discloses, further including adaptive circuitry, coupled to the second input of the second slicer, wherein the adaptive circuitry changes the second slicer level based on an upper edge and a lower edge of a receive eye of the second slicer (Paragraph 40 Lines 1-8 and Paragraph 44 Lines 1-11). Therefore, as discussed in claim 7 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include adaptive circuitry that changes the second slicer level based on an upper edge and a lower edge of a receive eye of the second slicer, as Little discloses, in the equalization circuitry of Tang et al., Ma et al., and Davis et al., in order to have a data slicer that is optimized for symbol detection.

7) Regarding claim 13:

Little further discloses, further including margining circuitry, coupled to the adaptive circuitry, wherein the margining circuitry determines the location of the upper inner edge and the lower inner edge of the receive eyes of the first and second slicer.

(Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the margining circuitry, the inner edges are interpreted as the upper and lower inner edges of the receive eye, and that it is easily concluded that location determination of first slicer edges by the margining circuitry is easily extrapolated to simultaneous location determination of second slicer edges).

8) Regarding claim 14:

Little further discloses, wherein the margining circuitry includes a margining slicer having a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the margining circuitry, and the mid point between inner edges is interpreted to be the margining slicer level).

9) Regarding claim 15:

Little further discloses, wherein the margining circuitry includes reference level adjustment circuitry to generate the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the reference level adjustment circuitry).

10)Regarding claim 16:

Little further discloses, wherein the reference level adjustment circuitry generates margining slicer levels that vary according to the margining algorithm (Block

640 in Figs. 6, 7 and Paragraph 44 Lines 1-11, wherein, it is clearly understood that the margining algorithm is executed by the adaptive slicer threshold generation system).

11)Regarding claim 17:

Ma et al. further discloses:

a first phase slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first phase slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level (Paragraph 7 Lines 1-5, wherein, one among the four paths of Fig. 1 through which signals a, b, c, and d pass is interpreted as the first data slicer, i.e., the first data detector).;

a second phase slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level (Paragraph 7 Lines 1-5, wherein, a second among the four paths of Fig. 1 through which signals a, b, c, and d pass is interpreted as the second data slicer, i.e., the second data detector);

margining circuitry to measure the value of an error signal of a phase sampling point (Paragraphs 25, 42, paragraph 43 lines 8-13 and 70 in Fig. 5, wherein, 70 in Fig. 5 is interpreted as the margining circuitry and the 'tracking error signal TES' is interpreted as the value of an error signal of a level sampling point).

It is desirable to change a phase slicer (detector) level based on the value of the phase error signal. Phase slicer (detector) level adjustment based on phase error results in optimized signal phase detection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the receiver of Tang et al., Davis et al., and Little a first and a second phase slicers (detectors) and to include a margining circuitry and an adaptive circuitry for, respectively, detecting phase error and adjusting slicer (detector) levels, as Ma et al. discloses, in order to result in the receiver having optimized signal phase detection.

Ma et al. does not disclose, adaptive circuitry, coupled to margining circuitry and the second input of the first slicer, wherein the adaptive circuitry changes the first slicer level based on the value of the error signal. However, as discussed in claim 6 above, Tang et al. discloses, adaptive circuitry, coupled to margining circuitry and the second input of the first slicer, wherein the adaptive circuitry changes the first slicer level based on the value of the error signal (Paragraph 16 Lines 4-7 and Paragraph 20 Lines 1-3, wherein, the offset generator is interpreted as the adaptive circuitry).

12)Regarding claim 18:

Little further discloses, wherein the margining circuitry includes a margining slicer having a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of the input symbol relative to the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is interpreted

to be the margining circuitry, and the mid point between inner edges is interpreted to be the margining slicer level).

13)Regarding claim 19:

Tang et al. discloses a receiver, coupled to a communications channel, to receive a plurality of input symbols transmitted by a transmitter, and to generate an output signal that is representative of each transmitted symbol (Paragraph 5 Lines 1-4 and Paragraph 16 Lines 3-4), the receiver comprising:

equalization circuitry, coupled to the communications channel to receive the plurality of input symbols (100 in Fig. 1), the equalization circuitry including:

a first data slicer having a plurality of inputs and an output, wherein a first input is adapted to receive the plurality of input symbols and a second input is adapted to receive a first slicer level, and wherein the first data slicer outputs a first or second value based on the amplitude of the input symbol relative to the first slicer level (120 in Fig. 1, Paragraph 17 Lines 1-4, Table 1 Page 2, Paragraphs 19 and 20);

a second data slicer having a plurality of inputs and an output, wherein a first input of the second data slicer is adapted to receive the plurality of input symbols and a second input of the second data slicer is adapted to receive a second slicer level, and wherein the second data slicer outputs the first or second value based on the amplitude of the input symbol relative to the second slicer level (130 in Fig. 1, Paragraph 17 Lines 1-4, Table 1 Page 2, Paragraphs 19 and 20);

logic circuitry, coupled to the first and second data slicers, to output a signal having either a first or second logic level wherein the first logic level is associated with

the first value and the second logic level is associated with the second logic level (140 in Fig. 1), and wherein:

if the data slicers output the same value, the logic circuitry outputs the logic level that is associated with the value output by the data slicers (Table 1 Page 2); and

if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol (Table 1 Page 2).

Tang et al. does not disclose margining circuitry, including at least one margining slicer, to determine the value of an error signal of a level sampling point. However, as discussed in claim 17 above, Ma et al. discloses margining circuitry, including at least one margining slicer, to determine the value of an error signal of a level sampling point (Paragraphs 25, 42, paragraph 43 lines 8-13 and 70 in Fig. 5, wherein, 70 in Fig. 5 is interpreted as the margining circuitry and the 'tracking error signal TES' is interpreted as the value of an error signal of a level sampling point)..

As discussed in claim 6 above, Tang et al. further discloses adaptive circuitry, coupled to the margining circuitry and the second input of the first data slicer, wherein the adaptive circuitry adjusts the first slicer level based on the at least one performance parameter (Paragraph 16 Lines 4-7 and Paragraph 20 Lines 1-3, wherein, the offset generator is interpreted as the adaptive circuitry and the offset value is interpreted as the one performance parameter).

14)Regarding claim 20:

Little, as discussed in claim 7 above, discloses, wherein the at least one performance parameter of the receiver includes an upper inner edge and a lower inner edge of a receive eye of the first data slicer (Paragraph 40 Lines 1-8 and Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the margining circuitry, and the inner edges are interpreted as the upper and lower inner edges of the receive eye).

15)Regarding claim 21:

Little, as discussed in claim 12 above, discloses wherein the at least one performance parameter of the receiver includes an upper edge and a lower edge of a receive eye of the second data slicer (Paragraph 40 Lines 1-8 and Paragraph 44 Lines 1-11).

16)Regarding claim 22:

Ma et al., as discussed in claim 17 above, discloses wherein the at least one performance parameter of the receiver includes error signal of a phase sampling point (Paragraph 7 Lines 1-5, Lines 22-25 and 37 in Fig. 2, wherein, phase difference produced by the phase difference detector is interpreted as the error signal).

17)Regarding claim 23:

Little discloses wherein the margining slicer includes a plurality of inputs and an output, wherein a first input of the margining slicer is adapted to receive the plurality of input symbols and a second input is adapted to receive a margining slicer level, and wherein the margining slicer outputs a first or second value based on the amplitude of

the input symbol relative to the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is interpreted to be the margining circuitry, and the mid point between inner edges is interpreted to be the margining slicer level).

18)Regarding claim 24:

Little discloses wherein the margining circuitry includes reference level adjustment circuitry to generate the margining slicer level (Paragraph 44 Lines 1-11, wherein, the threshold generation system is understood to be the reference level adjustment circuitry).

19)Regarding claim 25:

Little discloses wherein the reference level adjustment circuitry generates margining slicer levels that vary according to the margining algorithm (Block 640 in Figs. 6, 7 and Paragraph 44 Lines 1-11, wherein, it is clearly understood that the margining algorithm is executed by the adaptive slicer threshold generation system).

20)Regarding claim 26:

Tang et al. discloses the receiver of claim 19 wherein the first, second and margining data slicers each include a plurality of serially coupled sense amplifiers (Paragraph 17 Lines 4-6).

Conclusion

8. Applicant's amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Redman-White et al. (US Pub 2002/0021646) discloses an apparatus and a method for estimating input signal values at sampling instants in which a Viterbi decoder is utilized. Dagdeviren et al. (US Pub 2004/0120426) disclose a data recovery circuit comprising five distinct data slicers with locations at either the center or edge of the "eye" in the eye diagram of incoming data.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is

(571) 270-1075. The examiner can normally be reached Monday through Friday, 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi March 16, 2007

M. G

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER